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[Examples of contemporary VLIW CPUs include the TriMedia media processors by NXP \(formerly Philips Semiconductors\), the Super Harvard Architecture Single-Chip Computer \(SHARC\) DSP by Analog Devices, the C6000 digital signal processor \(DSP\) family by Texas Instruments, the ST200 family by STMicroelectronics based on the Lx architecture \(designed in Josh Fisher's HP lab by Paolo Faraboschi\), and the MPPA Manycore family by Kalray. These contemporary VLIW CPUs are mainly successful as embedded ...](#)

[Very long instruction word - Wikipedia](#)

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Microprocessor Architectures is cutting-edge text which will prove invaluable to both industrial hardware and software engineers involved in embedded system design and to postgraduate electrical engineering and computer science students. This clearly-structured reference demonstrates the versatility of TTAs and explores their influential role in the next generation of computer architecture.

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Microprocessor Architectures: From VLIW to Tta . 1997. Abstract. From the Publisher: The market for single chip microprocessors is huge and their performance continues to increase, driven by the on-going demand for more powerful applications, particularly in the control and signal processing domains. This work introduces a new type of computer ...

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Computer Architecture ABSTRACT VLIW architectures are distinct from traditional RISC and CISC architectures implemented in current mass-market microprocessors. It is important to distinguish instruction-set architecture—the processor programming model—from implementation—the physical chip and its characteristics. VLIW microprocessors and superscalar implementations of traditional

[An Introduction To Very-Long Instruction Word \(VLIW ...](#)

VLIW Architecture. Very-Long Instruction Word (VLIW) architectures are a suitable alternative for exploiting instruction-level parallelism (ILP) in programs, that is, for executing more than one basic (primitive) instruction at a time. These processors contain multiple functional units, fetch from the instruction cache a Very-Long Instruction Word containing several primitive instructions, and dispatch the entire VLIW for parallel execution.

[VLIW Architecture - IBM](#)

In computer architecture, a transport triggered architecture (TTA) is a kind of processor design in which programs directly control the internal transport buses of a processor. Computation happens as a side effect of data transports: writing data into a triggering port of a functional unit triggers the functional unit to start a computation. This is similar to what happens in a systolic array.

[Transport triggered architecture - Wikipedia](#)

Advantages of Superscalar Architecture : In a Superscalar Processor, the detrimental effect on performance of various hazards becomes even more pronounced. The compiler can avoid many hazards through judicious selection and ordering of instructions.

[Superscalar Architecture - GeeksforGeeks](#)

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WhatIs.com. Very long instruction word (VLIW) describes a computer processing architecture in which a language compiler or pre-processor breaks program instruction down into basic operations that can be performed by the processor in parallel (that is, at the same time). These operations are put into a very long instruction word which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit.

[What is VLIW \(very long instruction word\)? - Definition ...](#)

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[Superscalar & VLIW Architectures: Characteristics ...](#)

VLIW Introduction Superscalar Control Logic Scaling Each issued instruction must be checked against W\*L instructions, i.e., the growth in hardware ? W\*(W\*L) For in-order machines, L is related to pipeline latencies For out-of-order machines, L also includes time spent in instruction buffers (instruction window or ROB)