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To set up the Intel® Quartus® Prime software to run the Synplify software, do the following: On the Tools menu, click Options. In

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the Options dialog box, click EDA Tool Options and specify the path of the Synplify or Synplify Pro software under Location of Executable.

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Synplify Pro and Premier. Fast, Reliable FPGA Implementation and Debug. Overview. The Synopsys FPGA design tools are comprised of synthesis and debug tools that enable designers to quickly deliver competitive products to market with the lowest schedule risk. The Synplify synthesis tools provide fast runtime, performance, area optimization for cost and power reduction, multi-FPGA vendor support, incremental and team-design capabilities for faster FPGA design development.

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## Synplify Premier - Synopsys

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## Intel Quartus Prime Pro Edition User Guide

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## Synopsys FPGA Synthesis

- Synplify Premier tool to improve timing closure with Graph-based Physical Synthesis. Graph-based Physical Synthesis provides design stability, accurate timing correlation, minimal design iterations, and great timing performance. Single-Chip ASIC Verification Synplify Premier supports single-chip ASIC verification with:
  - Gated Clock Conversion

## Synplify Quick Start for Xilinx

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Synplify Pro ® Reference Manual February 2004 Synplicity, Inc.  
600 West California Avenue Sunnyvale, CA 94086 (U.S.) +1 408  
215-6000 direct (U.S.) +1 408 222-0263 fax

## Synplify Pro Reference Manual

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Modifications to cores generated by Coregen are not supported. For design or coding assistance, contact your Authorized Distributor or Sales Representative.

## Support - Xilinx

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To add to my last answer, you can refer to "Synopsys FPGA Synthesis User Guide" (fpga\_user\_guide.pdf) and search for Section "Incorporating Vivado IP". -vivian Don ' t forget to reply, kudo, and accept as solution.

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